Pira.cz **MRDS1322**

Basic Radio Data System Encoder MCU

DESCRIPTION

The MRDS1322 is a complete Radio Data System (RDS) encoder, configured via local onboard RS232 or I^2C bus. It implements physical and data-link layers and supports basic set of RDS services.

Internally the device is based on a programmable microcontroller. With a minimum of external parts it forms a simple RDS encoder add-on to analogue FM broadcast designs.

RDS SERVICES DIRECTLY SUPPORTED

- **PI** Program Identification
- **PS** Program Service
- **PTY** Program Type
- **TP** Traffic Program
- **AF** Alternative Frequencies
- **TA** Traffic Announcement
- **DI** Decoder Identification
- **M/S** Music/Speech
- **RT** Radiotext
- **UDG** User defined groups (2 modes)

CAPACITY

- AF: up to 15 items
- RT: 64 characters
- Dynamic PS text: up to 80 characters
- UDG: 2 groups (1 for each mode)

FEATURES

- Single supply 1.8 to 5.5 V
- Typical operating current: 7.9 mA @ 5.0 V
  5.6 mA @ 3.3 V
- Minimum external parts
- Industrial temperature range
- Internal EEPROM memory for data storage during power-off
- Support for external TA switch
- Indication LED output
- Both stereo and mono operation possible
- Digital 19 kHz pilot tone PLL with software phase shift adjustment
- Parallel 8-bit D/A converter, 361 kHz sampling rate (over-sampled)
- Broadcast quality output signal
- Only simple output filter required
- RDS/RBDS signal:
  conforms to CENELEC EN 50067 / EN 62106
- Continuous RDS transmission during all operations
- Communication bus for configuration purposes:
  Selectable RS232 or I^2C
  unidirectional or bi-directional operations
- RS232 baudrate: 2400 or 19200 Bd
  I^2C bus speed: DC to 400 kHz
- Selectable polarity of RS232 signal
- Buffered PS and UDG data
- 4 modes for dynamic/scrolling PS incl. word alignment and one-by-one character scrolling
- Windows control software, incl. free OEM
- RoHS compliant
- Packages available: 20-lead PDIP
  20-lead SOIC
  20-lead SSOP

APPLICATIONS

- Extremely low-cost FM broadcast RDS encoders
- Small all-in-one FM transmitters
- Private messaging systems
- RDS encoders for cable FM modulators
- Text output from any device to FM receiver

Revision 2023-06-02

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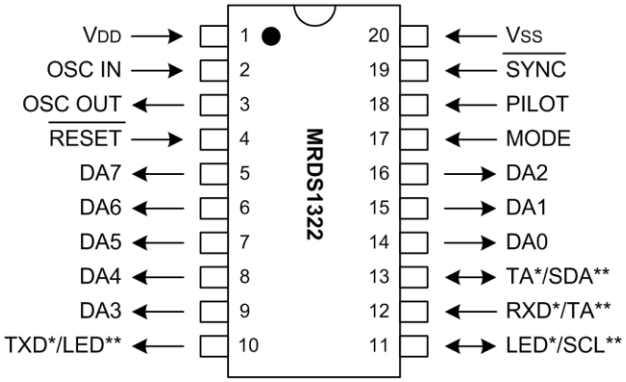
1 PIN DIAGRAMS AND DESCRIPTION



* Valid for RS232 mode / ** valid for I^2C mode.

Pin name	Description	Internal weak pull-up
/RESET	**Device reset** Logical low on this pin holds the device in reset state. If the reset function is not required, connect this pin to V_{DD} through a resistor.	
/SYNC	**Pilot sync. switch** Drive this pin low to confirm the pilot tone validity and to enable internal pilot PLL assuring stable phase relation between pilot tone and RDS sub-carrier. If the pilot sync. function is not required (mono or low power broadcast), leave this pin unconnected or connect it to V_{DD} through a resistor, so internal clock reference will be used.	✓
PILOT	**Pilot tone input** Optional 19 kHz pilot tone input for the synchronization purpose. If pilot tone is not available or does not meet the specifications required, the /SYNC pin should be driven high.	
TA	**TA switch** RDS Traffic Announcement (TA) flag control. If the TA external switching function is not required, leave this pin unconnected.	✓
V_{DD}	**Positive supply** Apply V_{DD} power supply voltage to this pin. Decoupling capacitor is required on V_{DD} and V_{SS} pins. A 100 nF 10-50V ceramic capacitor is recommended. The decoupling capacitor should be placed as close to the pins as possible.	
V_{SS}	**Ground reference**	

OSC IN	**Crystal oscillator input** Tie to 4.332 MHz crystal pin.	
OSC OUT	**Crystal oscillator output** Tie to 4.332 MHz crystal pin. Can be used for clocking another device on the board.	
LED	**Operation LED** Connect an indication LED (+) through a resistor or leave unconnected.	
MODE	**Communication mode** The MODE pin selects the communication mode. This pin is read by the device on power-up or after reset. Thus the MODE selection will not take effect until the next reset or power off-on cycle.	✓
SCL	**I^2C serial clock output** Open-drain terminal, external 2k pull-up resistor is required.	
SDA	**I^2C serial data input/output** Open-drain terminal, external 2k pull-up resistor is required.	
TXD	**Serial port transmit data** Serial RS-232 port transmit data output. Baud rate and signal polarity is selectable via the pin MODE.	
RXD	**Serial port receive data** Serial RS-232 port receive data input. Baud rate and signal polarity is selectable via the pin MODE.	
DA0-DA7	**D/A Converter bit 0 to 7** These pins together form a driving signal for the parallel D/A converter.	

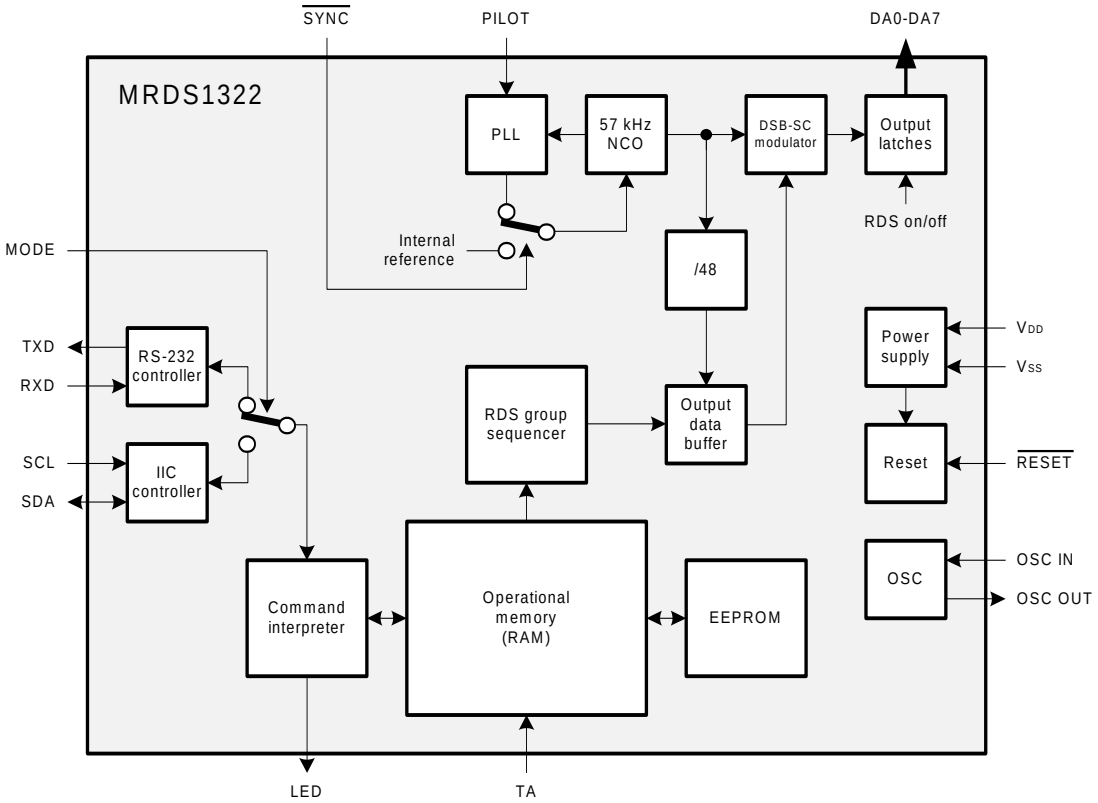


Figure 1.1 – Internal logical structure (simplified)

2 ELECTRICAL CHARACTERISTICS

Maximum Ratings

Ambient temperature under bias ..... -40 °C to +125 °C
Storage temperature ..... -65 °C to +150 °C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3 V to +6.0 V
Voltage on any I/O pin with respect to V_{SS} ..... -0.3 V to (V_{DD} + 0.3 V)
Maximum current sourced by any output pin ..... 25 mA
Maximum current sunk by any output pin ..... 25 mA

Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Supply voltage	1.8	-	5.5	V	
E_D	EEPROM Endurance	-	1M	-	E/W	-40 °C to +85 °C
F_{OSC}	Oscillator Frequency	-0.01 %	4.332	+0.01 %	MHz	* Note 1
F_S	D/A Converter sampling rate	-	361	-	kHz	
L_{PILOT}	Pilot tone level	150	-	V_{DD} - V_{SS}	mV pp	Stereo transmission
B_{PLL}	PLL capture range	-	8	-	Hz	
T_{PU}	Power-up delay	-	-	1100	ms	Mode 0, 1, 2
				140		Mode 3
F_{CLK}	I^2C clock frequency	0	-	400	kHz	Master supports clock stretching.
				20		Master ignores clock stretching.
T_{HIGH}	I^2C clock high time	600	-	-	ns	
T_{LOW}	I^2C clock low time	1300	-	-	ns	
T_{HD}/T_{SU}	I^2C hold/setup time	600	-	-	ns	
$T_{HD:DAT}$	I^2C data input hold time	0	-	-	ns	
$T_{SU:DAT}$	I^2C data input setup time	100	-	-	ns	
T_{AA}	I^2C output valid from clock	-	-	3500	ns	
T_{BUF}	I^2C bus free time	2400	-	-	µs	
		1000	-	-	ms	EEPROM store cmd.

* Note 1:

The crystal must oscillate on 4.332 MHz with tolerance of +/- 0.01 %. Depending on the crystal characteristics, the parallel capacitors (see section 3.2) may require change of their value for entire production batch. This should be tested on a sample before mass assembly.

The crystal frequency offset can be also read by a counter on the MRDS1322 pin 5 with the /SYNC pin left unconnected. The frequency read must be 57 kHz +/- 6 Hz.

Recommended crystal type is Auris **Q- 4,332000M-HC49US-F-30-30-D-16** or equivalent.

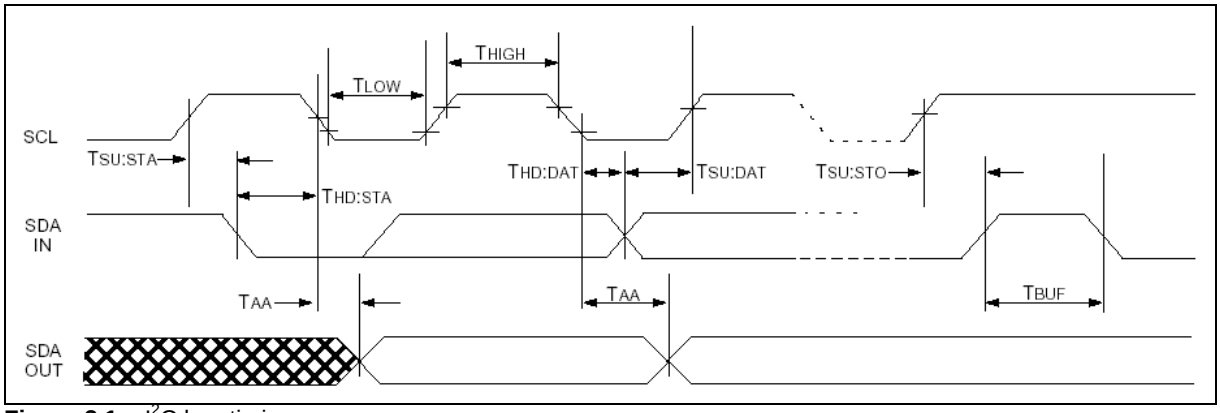


Figure 2.1 – I^2C bus timing

Supply Current (25 °C)

Supply voltage	**2.0 V**	**3.3 V**	**5.0 V**
Operating	3.6 mA	5.6 mA	7.9 mA
Subcarrier off	2.0 mA	3.7 mA	4.0 mA
Held in Reset	0.5 mA	0.9 mA	1.1 mA

2.1 Related Documents, Software and Development Support

Technical support is available through the web site at: http://pira.cz/rds/

The web site contains the following information: data sheets, application notes, sample programs, design resources, user's guides, latest software releases incl. Windows control software (TinyRDS, Magic RDS 4), Frequently Asked Questions (FAQ), online shop, online forum.

The most important links are listed below:

- FAQ: http://pira.cz/rds/show.asp?art=rds_encoder_support
- MicroRDS encoder & Windows control software: http://pira.cz/rds/show.asp?art=micrords_encoder
- MicroRDS Encoder - User Guide: http://pira.cz/rds/micrords.pdf
- Software development resource: http://pira.cz/rds/show.asp?art=micrords_development
- Pira.cz online shop: http://pira.cz/shop/

The MicroRDS encoder is based on the MRDS1322 chip. It is a sample design which implements everything needed to experience the MRDS1322 device.

3 CONNECTION DIAGRAMS AND APPLICATION NOTES

3.1 Device reset

A reset is generated by holding the /RESET pin low. The device has a noise filter in the reset path which detects and ignores small pulses.

A reset pulse is generated on-chip whenever V_{DD} rises above a certain threshold. This allows the device to start in the initialized state when V_{DD} is adequate for operation.

To take advantage of this feature, tie the /RESET pin through a resistor (1k to 10k) to V_{DD}. This will eliminate external RC components usually needed to create a reset delay.

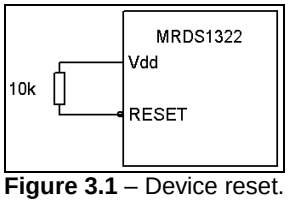


Figure 3.1 – Device reset.

When the device starts normal operation (i.e., exits the reset condition), device operating parameters (voltage, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

3.2 Crystal oscillator

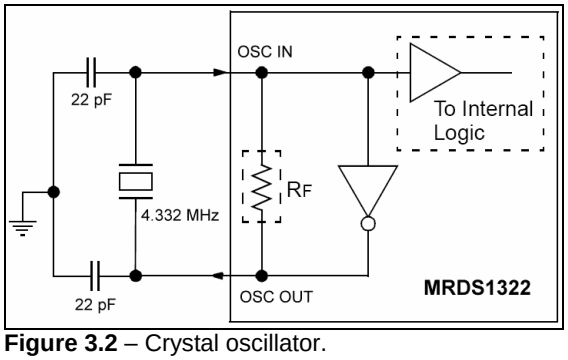


Figure 3.2 – Crystal oscillator.

3.3 Power supply

The power supply must be bypassed close to the device with a 100 nF ceramic capacitor. The device can operate within wide power supply voltage range (see the Electrical Specifications). The output RDS level varies proportionally to the supply voltage.

3.4 Internal PLL

The MRDS1322 includes an internal phase locked loop, which synchronises the RDS subcarrier with 19 kHz pilot tone in case of stereo broadcast. Parameters of the PLL are controlled by software.

Pilot tone is tied to the PILOT input pin. This pin includes an internal comparator with a threshold voltage of $V_{DD}/2$. Thus a pilot in TTL levels may be connected directly. For sine wave the DC component must be fixed at $V_{DD}/2$ using two resistors and coupling capacitor (figure 3.3).

The PLL is active if the /SYNC pin is driven low. This configuration makes easy to connect commonly available clock recovery circuits (LM567) if the pilot tone needs to be filtered from MPX signal.

The PLL should be permanently disabled (in case of mono transmission or if that function is not required) by leaving the /SYNC pin unconnected or connecting it to V_{DD} (directly or through a resistor).

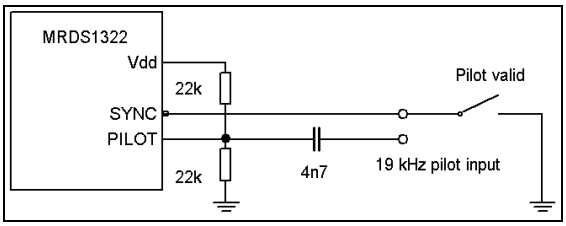


Figure 3.3 – Pilot input.

3.5 External TA switch

The external TA switch can set the Traffic Announcement flag to 1 if TP flag is on (1). The TA flag is set to 1 if the TA input is driven low. This can be done using simple mechanical switch (figure 3.4) or any logic circuit.

Where the external TA switch feature is not required, the TA pin may be left unconnected.

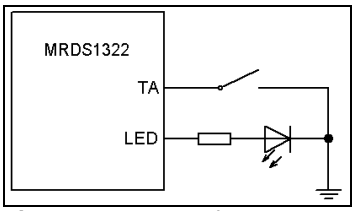


Figure 3.4 – TA and LED connection.

3.6 Operation LED

The LED indicates that the device is in operation. It blinks approx. once per second. It also indicates that data are being received through the communication interface (RS232 or I^2C bus).

3.7 Digital-to-Analog converter

The MRDS1322 uses parallel 8-bit D/A converter with over-sampling technique to generate the RDS signal modulated at 57 kHz subcarrier. Digital data provided on DAx pins can be directly formed into analogue output signal using an extremely low-cost resistor network.

Figure 3.7 shows a simple 6-bit D/A converter using six of binary weighted resistors. It contains one resistor for each bit of the DAC connected to a summing point. It's possible to add seventh resistor (62k) and form a 7-bit DAC.

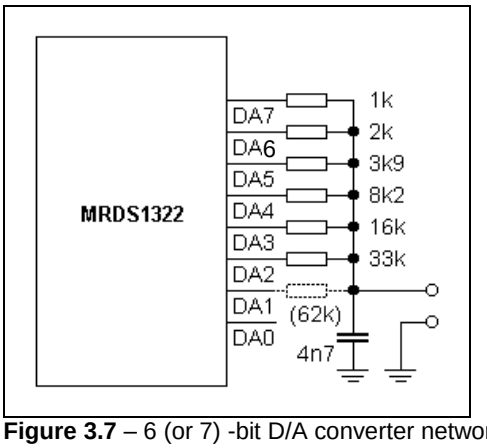


Figure 3.7 – 6 (or 7) -bit D/A converter network.

Figure 3.8 shows accurate 8-bit DAC using R/2R resistor network. It's a binary weighted DAC that creates each value with a repeating structure of 2 resistor values, R and R times two. This is an optimal DAC for this device.

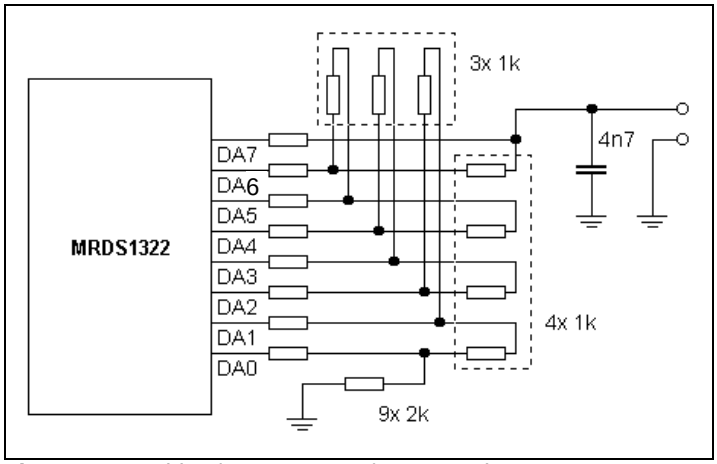


Figure 3.8 – 8-bit D/A converter R/2R network.

Below is a table showing typical values accomplished with each DAC type. The values are measured in base-band on FM transmitter input. 0 dBc corresponds to the RDS signal main spectral component at 57 kHz. 0 dB corresponds to 75 kHz peak FM deviation; peak deviation caused by RDS: 3.4 kHz.

Parameter	6-bit	7-bit	8-bit R/2R
57 kHz output signal bandwidth	+/- 2.4 kHz (43 dBc)	+/- 2.4 kHz (45 dBc)	+/- 2.4 kHz (50 dBc)
Spurious suppression	> 74 dB	> 80 dB	> 90 dB

Note: Typical signal-to-noise ratio of FM broadcast transmitters is 70 – 80 dB.

3.8 Output low-pass filter

The output RDS signal modulated at 57 kHz subcarrier requires no special filtering. Spurious products are kept below -70 dB broadcast limit and the D/A conversion residues around the sampling frequency can be cut-off using any simple low-pass filter. This may be based either on active filter or a simple LC element. For FM broadcast purposes the low-pass filter rejection should be at least 20 dBc on the sampling frequency. It is recommended for high quality FM broadcasting that the output filter characteristics interpolate at least these values:

15 kHz	57 kHz	360 kHz
-20 dBc	0 dBc	**-30 dBc**

4 COMMUNICATION MODE SELECTION

The device supports various communication modes for RDS data configuration. These modes cover all common methods of control including interfacing with mcu's, PC serial ports, USB adapters, Ethernet adapters, modems, etc. The communication protocol does not contain any security mechanism. If it is needed in your application, it must be assured by an upper layer.

The MODE pin selects the communication mode. This pin is read by the device on power-up or after reset. Some pins have different function, depending on the MODE selection (see section 1).

Mode No.	Description	Selection
0	RS232, 19200 Bd, active low (TTL)	Leave the MODE pin unconnected or connect it to V_{DD} MODE o——o Vdd
1	RS232, 19200 Bd, active high	Connect the MODE pin to DA2 pin through a diode MODE o—▷—o DA2
2	RS232, 2400 Bd, active low (TTL)	Connect the MODE pin to DA1 pin through a diode MODE o—▷—o DA1
3	I^2C Slave	Connect the MODE pin to V_{SS} MODE o——o Vss

4.1 Interfacing the MRDS1322

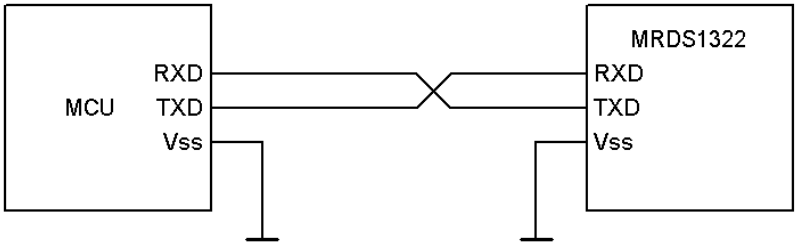


Figure 4.1 – Interfacing the MRDS1322 in mode 0 or 2.

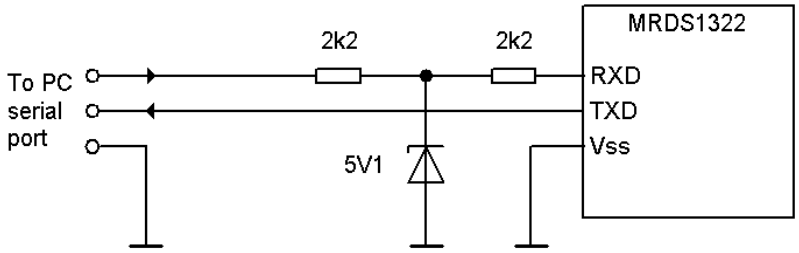


Figure 4.2 – Simple interfacing the MRDS1322 to a PC serial port in mode 1.

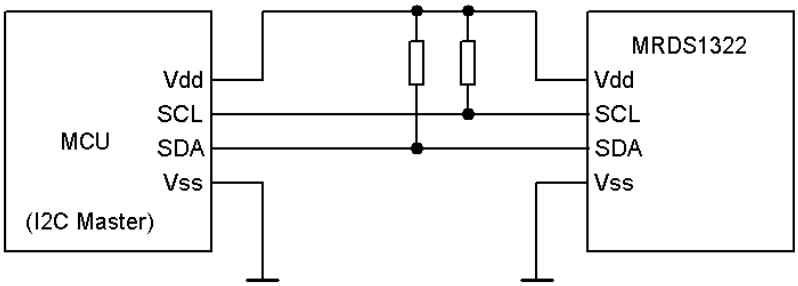


Figure 4.3 – Interfacing the MRDS1322 in mode 3.

5 I²C COMMUNICATION (MODE 3)

5.1 Bus specification

The I²C is a bi-directional bus used to transfer addresses and data into and out of the device. According to the bus specification the MRDS1322 is a slave device driven by master. The master generates clock signal, START/STOP conditions, addresses and specifies if read or write operation will be performed. All devices on the I²C bus are open drain terminals, therefore the bus requires pull-up resistors to V_{DD}.

The I²C peripheral implemented in the MRDS1322 fully meets the I²C specification with respect to the bus timing specified in section 2. **The application developer may apply the same routines and libraries like for the communication with standard serial I²C EEPROM's** (for example 24LC04). Configuration of the RDS transmission is made by writing values to address locations as showed in section 7.

5.2 Write operations

All write operations are performed in RAM so the number of write operations is unlimited. Storing the data into internal EEPROM memory is activated by a special command – writing a special value to the CONTROL register. Number of bytes written in page write mode is limited only by access RAM boundaries. For safety purposes the internal address counter will not wrap around if the last byte accessible is overstepped.

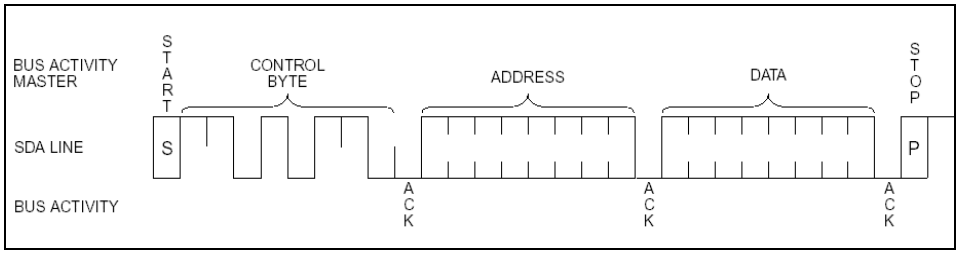


Figure 5.1 – Byte write

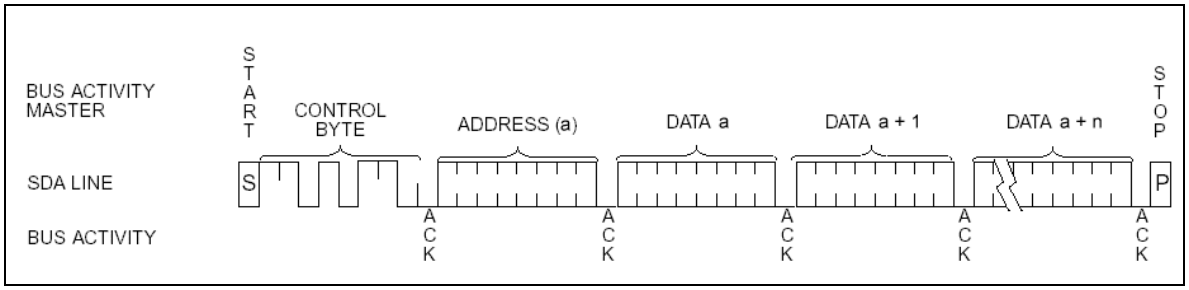


Figure 5.2 – Page write

5.3 Read operations

Read operations allow the master to access any RAM location. Implementation of the read operations is optional. To perform the read operation, first the word address must be set. This is done by sending the word address to the device as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a one.

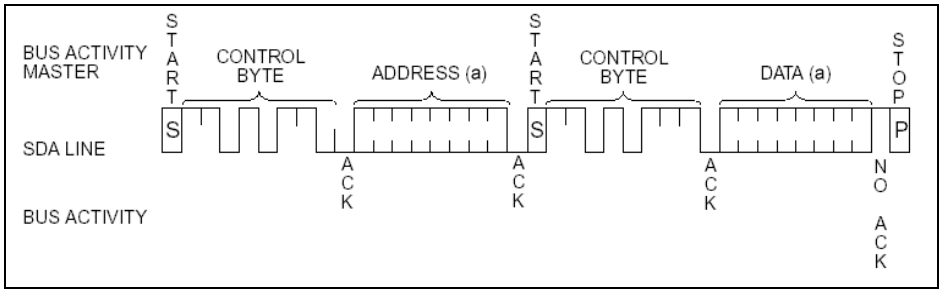


Figure 5.3 – Random read

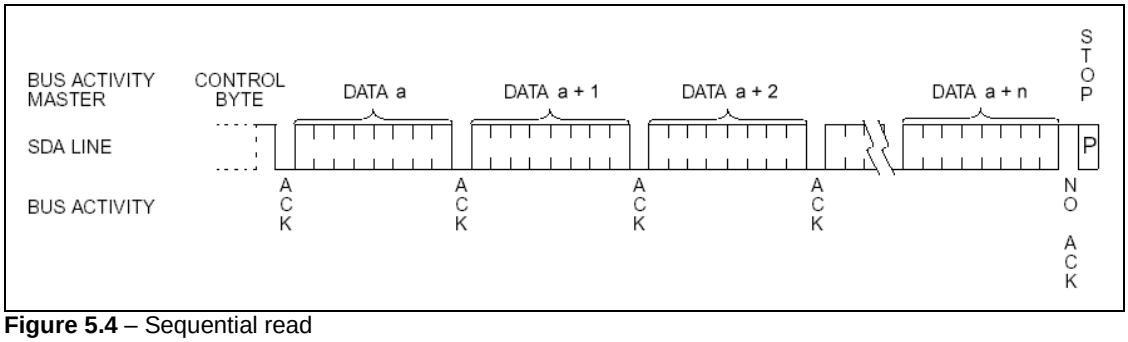


Figure 5.4 – Sequential read

5.4 Control byte

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 7-bit control code. For the MRDS1322 this is set as 1101011 binary for read and write operations. The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

Operation	Control byte	
	Control code	R/W
Write	1101011	0
Read	1101011	1

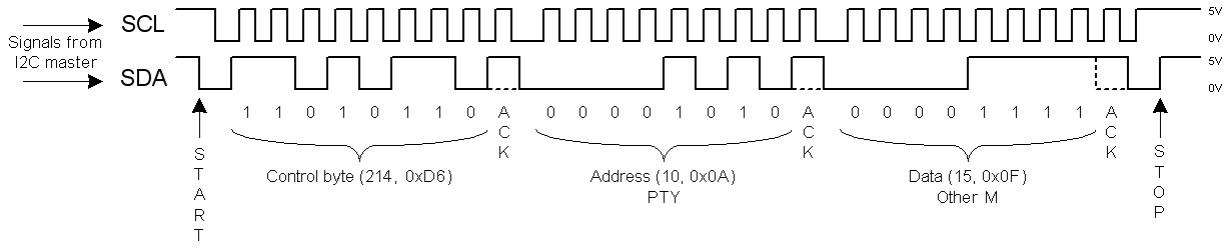
5.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge (ACK) after the reception of each byte (9th bit). The master device must generate an extra clock pulse which is associated with this acknowledge bit. The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

5.6 Clock stretching

A slave causes the SCL pin to be held low at the end of each data receive sequence. By holding the SCL line low, the slave has a time to process the last byte received before the master initiates another data transfer sequence. This enables the master to use high SCL frequency and prevents data lost due to possible overrun in the slave.

5.7 Application example (setting PTY)



More about I²C:

[1] – The I²C Bus Specification; Philips Semiconductors, www.nxp.com
[2] – 24LC04B/08B I²C Serial EEPROM's datasheet; Microchip, www.microchip.com

6 RS232 COMMUNICATION (MODE 0, 1, 2)

For the RS232 communication, any write or read command as well as the data read comprise of a series of bytes, delimited by two reserved bytes (start byte and stop byte), which mark the beginning and end of the block.
The start and stop bytes are uniquely defined, and may not occur within the block. In order to prevent this, the data is byte-stuffed prior to transmission. Byte-stuffing transforms an illegal occurrence of a reserved byte into two legal bytes. The reverse process is applied at read operation, byte-stuffed data are converted prior to processing. Thus, although the start and stop bytes are reserved, the data may contain bytes with any value.

6.1 Write operations

Each write command contains a start address pointing to the first location written in the device memory. No response is sent back. Thus the TXD pin may be left unconnected.

Start byte **0xFE**	Start address	Data	Stop byte **0xFF**

Figure 4.1 – Write command format

6.2 Read operations

Each read command contains a read constant (0xD0), start address pointing to the first location read and length of the data read.

Start byte **0xFE**	Read constant **0xD0**	Start address	Length	Stop byte **0xFF**

Figure 4.2 – Read command format

Start byte **0xFE**	Start address	Data	Stop byte **0xFF**

Figure 4.3 – Response format

6.3 Byte stuffing

The technique of byte-stuffing is achieved by trapping reserved bytes in illegal fields, and transforming them into legal byte pairs. Byte values 0xFD, 0xFE, and 0xFF are transformed into a pair of bytes as shown in the table.

Byte	Transformed into
0xFD	0xFD 0x00
0xFE	0xFD 0x01
0xFF	0xFD 0x02

Thus, the bytes reserved for start and stop conditions (0xFE and 0xFF) will never occur within the block.

6.4 Application example (setting PI to 30FF and reading it back for verify)

To set the PI: FE 00 30 FD 02 FF →
To read the PI: FE D0 00 02 FF →
The response received: FE 00 30 FD 02 FF ←

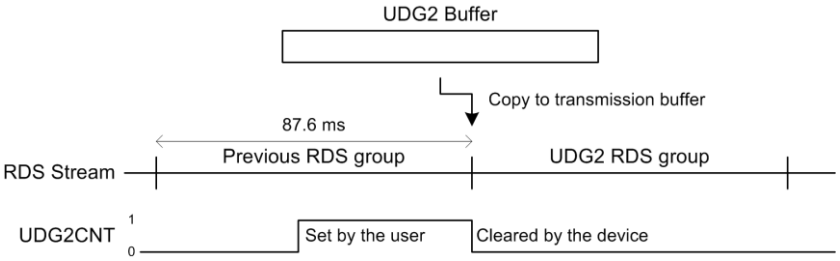
6.5 Firmware update

To allow firmware update, the final equipment must provide the RS232 interface and must allow to be set to one of the modes 0, 1 or 2. The firmware update is realised using a specialized Windows application. Currently (2016) no firmware update has been released yet.

7 COMMENTED MEMORY MAP

Address		Parameter	Description
HEX	DEC		
00-01	0-1	PI	Program Identification code. Identification code of the radio station. Always contains four hexadecimal digits.
02-09	2-9	PS Buffer	Program Service name (buffered). Static name of radio station that is displayed on receiver. Max. 8 characters long, redundant characters must be filled as spaces (32). Writing to this region is synchronized with the group order in order to provide the best visual result on most receivers.
0A	10	PTY	Program Type (0-31). An identification number to be transmitted with each program item, intended to specify the current Program Type within 32 possibilities. Program type codes (Europe / US): 0 – (none) / (none) 1 – News / News 2 – Affairs / Information 3 – Info / Sports 4 – Sport / Talk 5 – Education / Rock 6 – Drama / Classic Rock 7 – Cultures / Adult Hits 8 – Science / Soft Rock 9 – Varied Speech / Top 40 10 – Pop Music / Country 11 – Rock Music / Oldies 12 – Easy Music / Soft 13 – Light Classics Music / Nostalgia 14 – Serious Classics / Jazz 15 – Other Music / Classical 16 – Weather / Rhythm and Blues 17 – Finance / Soft Rhythm and Blues 18 – Children / Foreign Language 19 – Social Affairs / Religious Music 20 – Religion / Religious Talk 21 – Phone In / Personality 22 – Travel / Public 23 – Leisure / College 24 – Jazz Music / (unassigned) 25 – Country Music / (unassigned) 26 – National Music / (unassigned) 27 – Oldies Music / (unassigned) 28 – Folk Music / (unassigned) 29 – Documentary / Weather 30 – Alarm Test / Emergency Test 31 – Alarm / Emergency
0B	11	DI	Decoder Identification (0-15).
0C	12	MS	Music/Speech switch (0/1). 0 – Speech program 1 – Music program
0D	13	TP	Traffic Program (0/1). This is a flag to indicate that the tuned program carries traffic announcements. The TP flag must only be set on programs that dynamically switch on the TA identification during traffic announcements. The signal shall be taken into account during automatic search tuning.

0E	14	TA	Traffic Announcement (0/1). Indicates instantaneous presence (1) of traffic information during broadcasting. When this value is set to 1 by external TA switch, the value specified by TA command has no effect. When this value is set to 1 by TA command, the value set by external TA switch has no effect.
0F	15	AFNUM	Number of Alternative Frequencies (0-15).
10-1E	16-30	AF	List of Alternative Frequency channels in hexadecimal range of 01-CC (87.6-107.9 MHz). Up to 15 items allowed. Starts at the first address.
1F	31	RTEN	Bit 0: Enables (1) or disables (0) the Radiotext. Bit 1: Controls the RT A/B type flag.
20-5F	32-95	RT	Radiotext. Up to 64 characters long text message to be displayed on receiver in Radiotext format. Redundant characters must be filled as spaces (32). Car radios usually don't support this service, Dynamic PS can be used instead.
60	96	UDG1EN	Enables (1) or disables (0) the UDG1 transmission. By default (if RT is enabled), the group order on the device output is 0A 0A 0A 0A 2A (UDG1) 0A 0A 0A 0A 2A (UDG1) etc.
61-66	97-102	UDG1 Buffer	User Defined Group 1 (buffered) Specifies one free content group in BBBBCCCCDDDD format, which is repeatedly transmitted by the RDS encoder. BBBB, CCCC and DDDD represent the contents of the block B, block C and block D. The RDS encoder calculates the CRC automatically. According to the RDS standard, the block A has not been specified as it is always the PI code. According to the RDS standard, the block C is internally substituted by the PI code whenever block B bit 11 is set to 1, indicating group version *B*. The PTY and TP services set in the UDG1 group (block B bits 10:5) are ignored and are substituted according to the internal configuration of these services in the RDS encoder.
67-6C	103-108	UDG2 Buffer	User Defined Group 2 (buffered) Orders the RDS encoder to send directly RDS group whose content is free. The Group content is in BBBBCCCCDDDD format where BBBB, CCCC and DDDD represent the contents of the block B, block C and block D. The RDS encoder calculates the CRC automatically. According to the RDS standard, the block A has not been specified as it is always the PI code. According to the RDS standard, the block C is internally substituted by the PI code whenever block B bit 11 is set to 1, indicating group version *B*. The PTY and TP services set in the UDG2 group (block B bits 10:5) are ignored and are substituted according to the internal configuration of these services in the RDS encoder. Using this command, the RDS transmission can then be partially or fully controlled by an external application.

6D	109	UDG2CNT	Can be set to 0-8. When set to a value greater than zero, the UDG2 group starts to be inserted from the buffer to the RDS stream. Each transmission will decrease the UDG2CNT byte by 1. When the value counts down to zero, the UDG2 transmission will stop in the next cycle. The buffer content will retain.  **Figure 7.1** – Inserting one UDG2 RDS group When the UDG2CNT is decrementing, the UDG2 groups make a continuous block on the output. Changing the buffer content while the UDG2CNT is greater than zero is not allowed. If high UDG rate is required, the user may read the UDG2CNT byte and test it for zero value in order to recognize that another group can be written to the UDG2 buffer. This allows for fully synchronous UDG transmission.
6E	110	EXTSYNC	External pilot synchronisation. 1 – Automatic external synchronisation if pilot tone present (default) 0 – Forced internal clock source (for mono transmission only)
6F	111	PHASE	RDS Signal phase (0-18). Fixes the relative phase shift between the pilot tone and the RDS signal. Has effect only if bit 0 of the EXTSYNC is set to 1 and pilot tone is present. Changing the value by one results in 9.5 degrees phase shift change. The value serves only as a scale, it may not provide real phase shift value.
70	112	**STATUS**	Status register – **read only**. Bit 0: 1 – Pilot tone present 0 – Pilot tone not present or internal clock source set Bit 1: State of TA that is on air. Bit 2: Indicates if Dynamic PS text loop is running (1) or static PS is displayed (0). Bit 3: Indicates whether the new PS is still waiting in the PS buffer (1) or the PS buffer content has been already copied (0). Bit 7: Indicates whether the RDS subcarrier is on (1) or off (0).
71	113	**CONTROL**	Control register – **write only**. Depending on the value written the operation is performed. 69 (0x45, ‘E’): Stores all RAM content to internal EEPROM. The content will be restored on next power-up. 82 (0x52, ‘R’): Provokes a hardware reset of the RDS encoder and is equivalent to an "off-on" cycle of the RDS encoder. Must be the only byte written in the START-STOP session. 48 (0x30, ‘0’): Switches off the RDS subcarrier. Must be the only byte written in the START-STOP session. 49 (0x31, ‘1’): Switches on the RDS subcarrier.
72	114	SPSPER	Static PS period (0-255). Specifies the time between two repeats of the Dynamic PS text. Static PS (PS) is displayed during this time. Increasing the value by 1 increases the period by approx. 2.7 seconds. If value 255 is set, the Dynamic PS will be displayed only once, if the DPSNUM address is written.

73	115	DPSMOD	Display mode for the Dynamic PS text (0-3). 0 – Scrolling by fixed 8 characters 1 – Scrolling by 1 character 2 – Word alignment scrolling 3 – Scrolling by 1 character, text separated by spaces at begin and end *The dynamic PS text must be longer than 7 characters for mode **1**.*
74	116	LABPER	Label period in range of 0-255 used in Dynamic PS mode 0 and 2. Increasing the value by 1 increases the period by approx. 0.54 seconds.
75	117	SCRLSPD	Scrolling PS speed (0/1). Sets high (0) or low (1) speed of scrolling PS transmission (mode 1 and 3). Although setting high speed gives the result looking better, remember that on some receivers or under bad reception conditions the text may be unreadable. The reason has nothing to do with the device and comes out from the fact that scrolling PS has never been included in the RDS standard.
76	118	DPSNUM	Number of characters in Dynamic PS (0-80). When written, the Dynamic PS text loop restarts.
77-C6	119-198	DPS	Dynamic PS. Up to 80 characters long text message to be displayed on receiver instead of static PS name. Can be used for song titles streaming etc. Before writing new text, set the DPSNUM to 0. After the text is written, set the DPSNUM to corresponding value.
C7	199		*(reserved)*
C8-CF	200-207	PS	Program Service name (not buffered).

Notes:

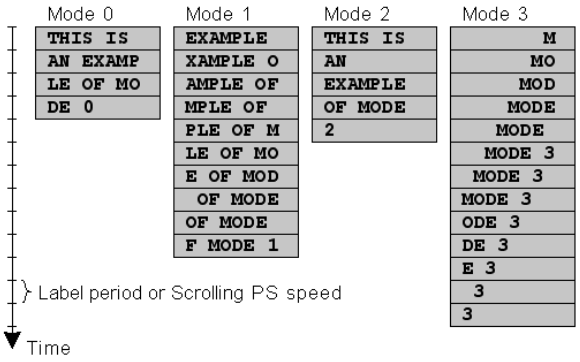
- Buffered address range – Content of this address range is not directly used for the RDS transmission. If at least one byte from the address range is written, after STOP condition on the bus the content is copied to internal not buffered address range and synchronised with RDS groups order. This prevents transmission of partial content and mixing old and new strings when the address range is written. For the PS both buffered and not buffered address ranges are provided.

- Bit order:

MSB LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

- Dynamic PS examples for each DPSMOD value:



- UDG1 and UDG2 byte order in the block: Higher byte is sent first.

- Application note for general purpose data transmission using UDG groups: It is possible to use last 4 bytes (block C and D) for general purpose data transfers. Longer data may split into 4 bytes segments, sent in sequence. The sequence counter can be put into block B bits 4:0. The group type (block B bits 15:11) should be set to 01100.

8 TEST CIRCUIT

8.1 Schematic diagram

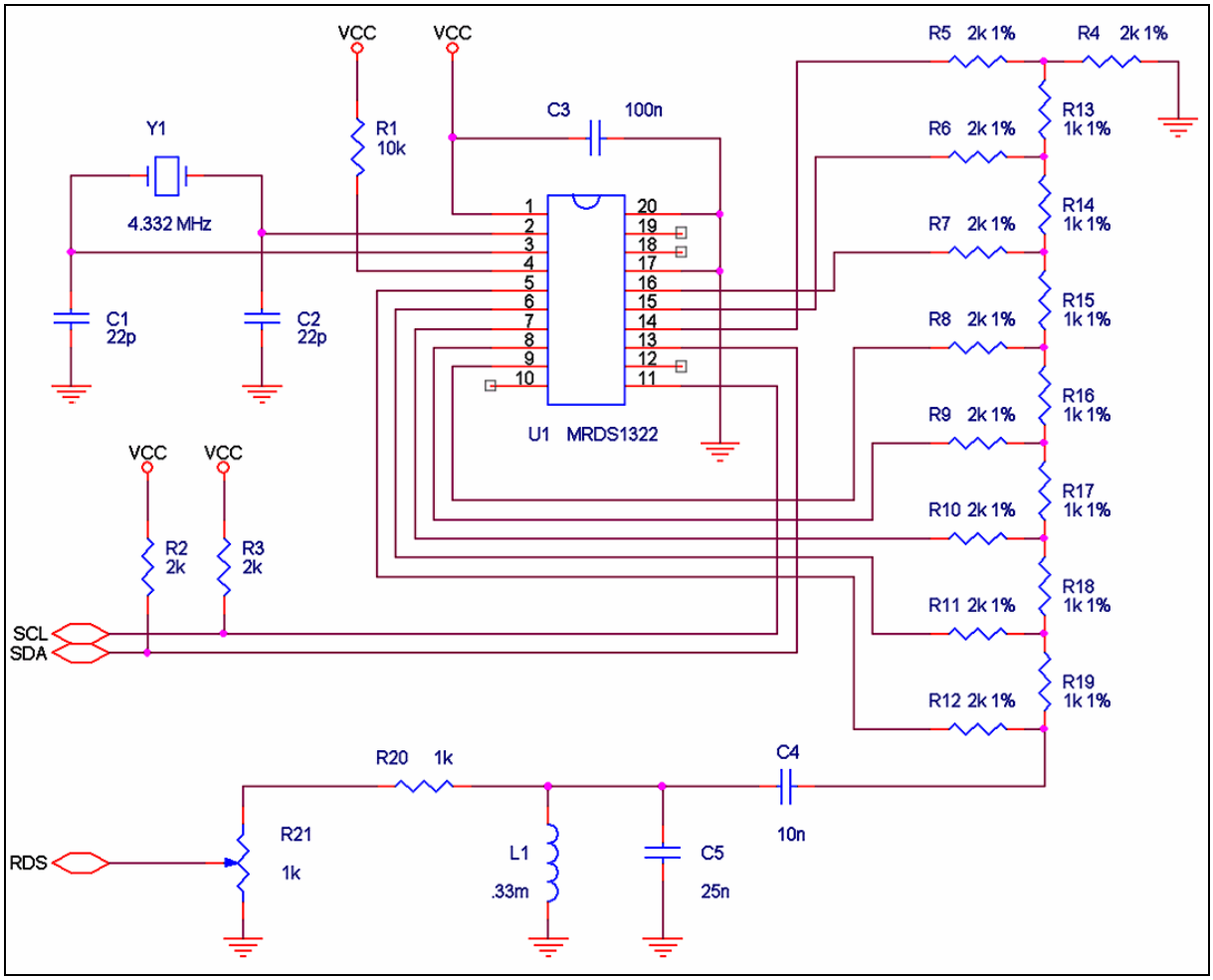


Figure 8.1 – Test circuit schematic diagram.

8.2 Characteristics

The test circuit is characterized as follows:

- Power supply voltage: 5 V
- Communication bus: I^2C
- DAC type: R/2R 8-bit
- Output filter: simple LC element resonating at 57 kHz (L1 serial resistance 1.9 Ω; C5 is a plastic film type, a value of 25 nF has been chosen to compensate the L1 inductance loss at higher frequencies)
- Output level: adjustable 0 to 1 V pp
- LED output, TA input: not used
- Pilot input: not used (switched to internal reference)

8.3 Output analysis

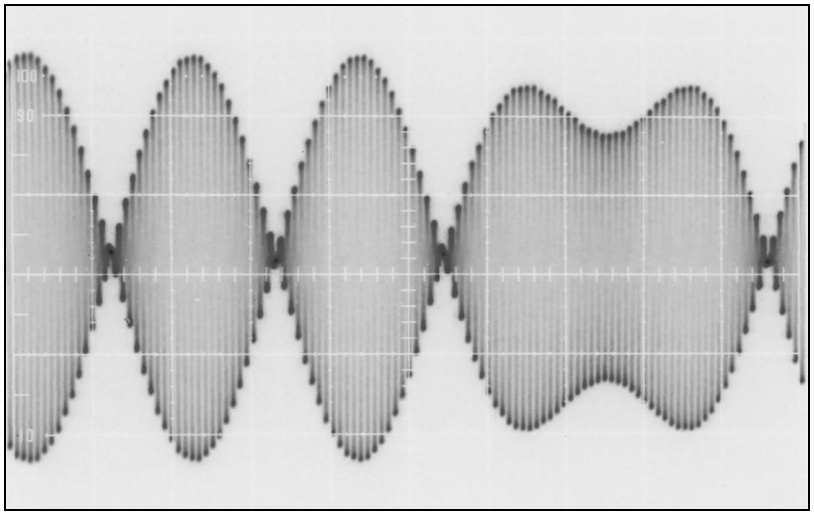


Figure 8.2 – Output RDS signal on oscilloscope (horizontal: 200 µs/div, vertical: 200 mV/div).

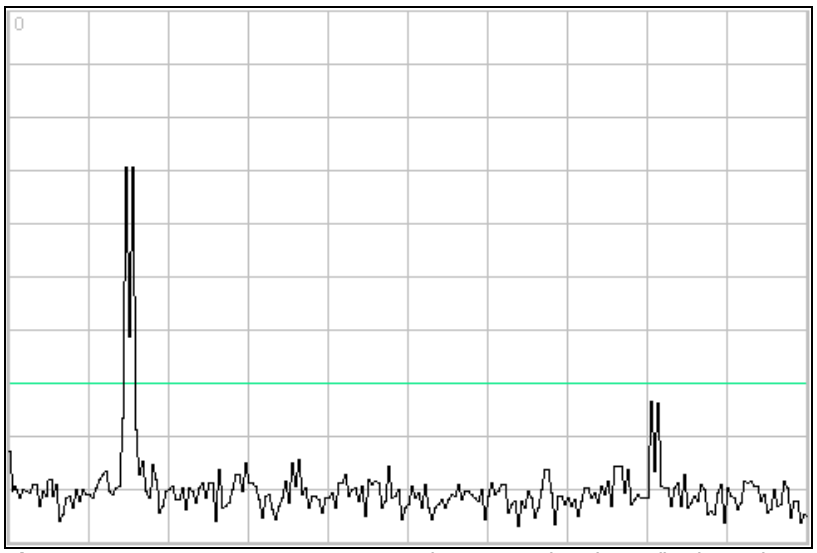


Figure 8.3 – Output spectrum measured on transmitter input (horizontal: 37.5 kHz/div, vertical: -10 dB/div; 0 dB corresponds to 75 kHz peak FM deviation; peak deviation caused by RDS: 3.4 kHz).

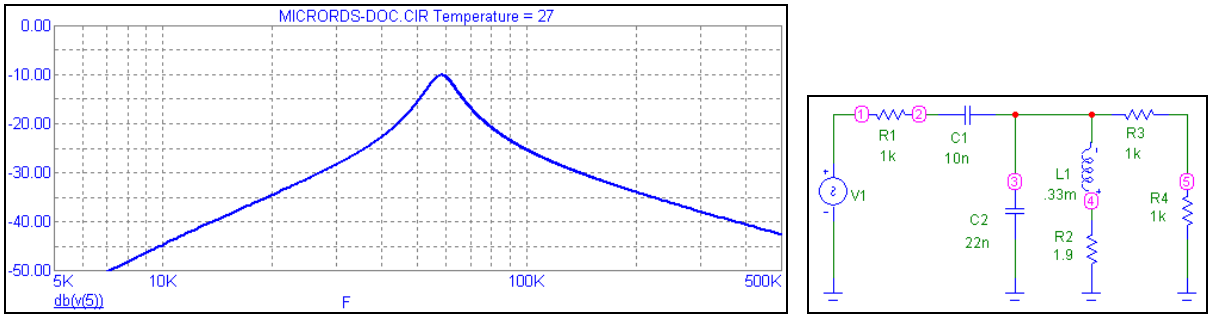
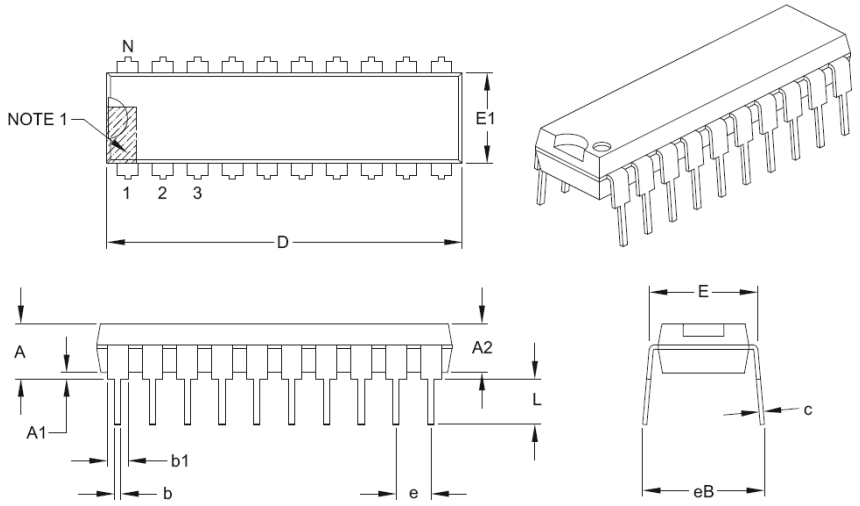


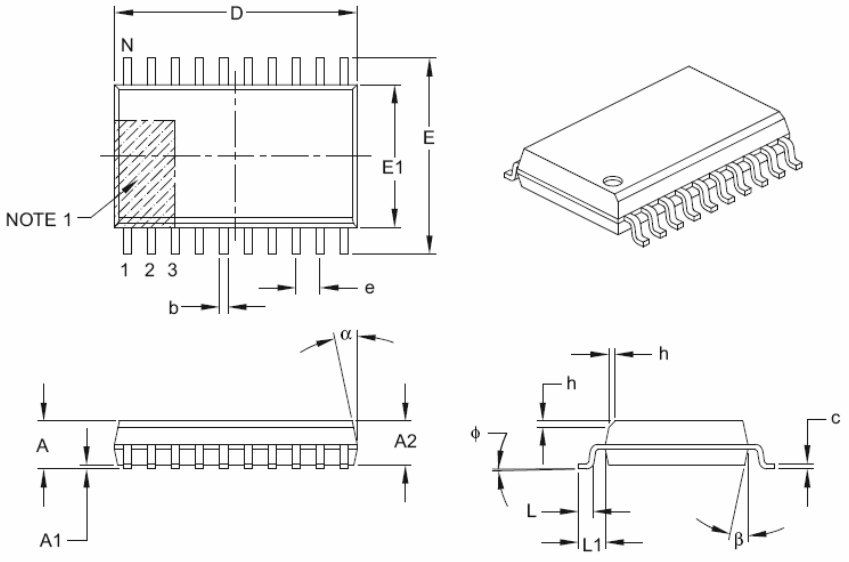
Figure 8.4, 8.5 – Output LC filter characteristics.

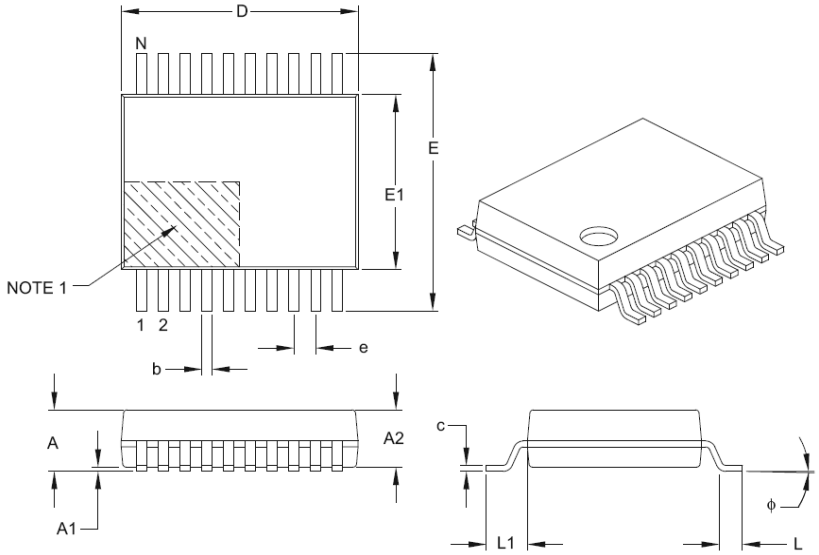
9 PACKAGE DETAILS



20-Lead PDIP – 300 mil Body			
Symbol	MIN	NOM	MAX
N		20	
e		.100 BSC	
A	-	-	.210
A2	.115	.130	.195
A1	.015	-	-
E	.300	.310	.325
E1	.240	.250	.280
D	.980	1.030	1.060
L	.115	.130	.150
c	.008	.010	.015
b1	.045	.060	.070
b	.014	.018	.022
eB	-	-	.430

20-Lead SOIC – 7.5 mm Body			
Symbol	MIN	NOM	MAX
N		20	
e		1.27 BSC	
A	-	-	2.65
A2	2.05	-	-
A1	0.10	-	0.30
E		10.30 BSC	
E1		7.5 BSC	
D		12.80 BSC	
h	.25	-	0.75
L	.40	-	1.27
L1		1.40 REF	
Φ	0°	-	8°
c	0.20	-	0.33
b	0.31	-	0.51
α	5°	-	15°
β	5°	-	15°





20-Lead SSOP – 5.30 mm Body			
Symbol	MIN	NOM	MAX
N		20	
e		0.65 BSC	
A	-	-	2.00
A2	1.65	1.75	1.85
A1	0.05	-	-
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
D	6.90	7.20	7.50
L	.55	0.75	0.95
L1		1.25 REF	
Φ	0°	4°	8°
c	0.09	-	0.25
b	0.22	-	0.38

Note 1: Pin 1 visual index feature may vary, but must be located within the hatched area.